CLAIMS

What is claimed is:

1. A method of input offset voltage compensation in a bipolar transistor differential amplifier having resistive loads on the bipolar transistor differential input pair comprising:

biasing the differential input pair with a bias current proportional to absolute temperature;

splitting the resistive loads into series combinations of a primary resistance and a trim resistance;

coupling a trim current source output to a trim resistances, the trim current source comprising a plurality of proportional to absolute temperature current source components individually controllably switchable to the trim current source output, each contributing a respective trim current component to the trim current source in a binary progression; and,

switching selected proportional to absolute temperature current source components to the trim current source output to minimize the input offset voltage of the differential amplifier.

2. The method of claim 1 wherein the plurality of proportional to absolute temperature current source

components are equal current components proportional to the current biasing the differential input pair, each current source component being switchable to a respective node of an R-2R network.

3. The method of claim 2 wherein switching selected proportional to absolute temperature current source components to the trim current source comprises loading a switch control word into a control register, each bit of the control word controlling a respective switch.

4. The method of claim 3 wherein the control word is provided through a digital interface.

5. The method of claim 1 further comprised of coupling the trim current source output to a predetermined one of the trim resistances, coupling a crossover switch in series with the resistive loads, and controlling the crossover switch to predetermine which trim resistance requires trim current for input offset voltage compensation.

6. The method of claim 1 wherein the differential amplifier includes a symmetrical high gain second stage and further comprising biasing the second stage with a constant current.

7. The method of claim 1 wherein the differential amplifier includes a symmetrical high gain second stage and further comprising biasing the second stage with a current proportional to absolute temperature.

8. A method of input offset voltage compensation in a bipolar transistor differential amplifier having resistive loads on the bipolar transistor differential input pair comprising:

biasing the differential input pair with a bias current proportional to absolute temperature;

coupling a trim current source output to at least one of the resistive loads, the trim current source comprising a plurality of proportional to absolute temperature current source components individually controllably switchable to the trim current source output; and,

switching selected proportional to absolute temperature current source components to the trim current source output to minimize the input offset voltage of the differential amplifier.

9. The method of claim 8 wherein switching selected proportional to absolute temperature current source components to the trim current source comprises loading a

switch control word into a control register, each bit of the control word controlling a respective switch.

10. The method of claim 9 wherein the control word is provided through a digital interface.

11. The method of claim 8 further comprising splitting the resistive loads into series combinations of a primary resistance and a trim resistance, and coupling the trim current source output to at least one of the trim resistances.

12. The method of claim 8 wherein the proportional to absolute temperature current source components contribute respective trim current components to the trim current source in a binary progression.

13. The method of claim 12 wherein the plurality of proportional to absolute temperature current source components are equal current components proportional to the current biasing the differential input pair, each being switchable to a respective node of an R-2R network.

14. The method of claim 8 further comprised of coupling a crossover switch in series with the resistive loads and controlling the crossover switch to predetermine the initial polarity of the input offset voltage to be compensated.

15. The method of claim 8 wherein the differential amplifier includes a symmetrical high gain second stage and further comprising biasing the second stage with a constant current.

16. The method of claim 8 wherein the differential amplifier includes a symmetrical high gain second stage and further comprising biasing the second stage with a current proportional to absolute temperature.

17. In a bipolar transistor differential amplifier, the improvement comprising:

a bipolar transistor differential input pair, each transistor having as a load a series combination of a primary resistance and a trim resistance;

a proportional to absolute temperature current source biasing the differential input pair; and,

a trim current source having an output coupled to at least one of the trim resistances, the trim current source comprising a plurality of proportional to absolute temperature current source components individually controllably switchable to the trim current source output, each contributing a respective trim current component to the trim current source in a binary progression.

18. The improvement of claim 17 further comprising an R-2R network and wherein the plurality of proportional to absolute temperature current source components are equal current components proportional to the current biasing the differential input pair, each being switchable to a respective node of the R-2R network.

19. The improvement of claim 18 further comprising a register holding a control word controlling the switching of individual proportional to absolute temperature current source components.

20. The improvement of claim 19 further comprising a digital interface coupled to the register for inputting a control word to the register.

21. The improvement of claim 17 further comprised of a crossover switch in series with the resistive loads, a control word in the control register also controlling the crossover switch.

22. The improvement of claim 17 further comprising a symmetrical high gain second stage biased with a constant current.

23. The improvement of claim 17 further comprising a symmetrical high gain second stage biased with a current proportional to absolute temperature.

24. In a bipolar transistor differential amplifier, the improvement comprising:

a bipolar transistor differential input pair, each transistor having a resistive load;

a proportional to absolute temperature current source biasing the differential input pair; and,

a trim current source having an output coupled to at least one of the resistive loads, the trim current source comprising a plurality of proportional to absolute temperature current source components individually controllably switchable to the trim current source output, each contributing a respective trim current component to the trim current source.

25. The improvement of claim 24 further comprising a register holding a control word controlling the switching of individual proportional to absolute temperature current source components.

26. The improvement of claim 25 further comprising a digital interface coupled to the register for inputting a control word to the register.

27. The improvement of claim 24 wherein at least one resistive load comprises a series combination of a primary resistance and a trim resistance, the trim current source output being coupled to at least one of the trim resistances.

28. The improvement of claim 24 wherein the proportional to absolute temperature current source components each contribute a respective trim current component to the trim current source in a binary progression.

29. The improvement of claim 24 further comprising an R-2R network and wherein the plurality of proportional to absolute temperature current source components are equal current components proportional to the current biasing the differential input pair, each being switchable to a respective node of the R-2R network.

30. The improvement of claim 24 further comprised of a crossover switch in series with the resistive loads and controlling the crossover switch to predetermine which resistive load is coupled to which compensated bipolar transistor.

31. The improvement of claim 24 further comprising a symmetrical high gain second stage biased with a constant current.

32. The improvement of claim 24 further comprising a symmetrical high gain second stage biased with a current proportional to absolute temperature.